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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,656	02/09/2004	Yoshihisa Yamashita	10873.1397US01	1445

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EXAMINER	
DINH, TUAN T	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,656	YAMASHITA ET AL.	
	Examiner	Art Unit	
	Tuan T. Dinh	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakatani et al. (6,038,133) in view of Ozawa et al. (U.S. Patent 5,172,304).

As to claims 1, 15-16, Nakatani et al. discloses an electronic component built-in module as show in figures 1-6 comprising:

a pair of opposed circuit substrates (401a, c, see figure 4), each of which includes a wiring pattern (402) and an insulating base material containing a resin (401);

an insulating layer (element 401 of insulating substrate 401b) that is placed between the pair of circuit substrates and contains an inorganic filler and a resin composition containing a thermosetting resin (see column 11, lines 24-25);

at least one electronic component (403) that is embedded and housed in the insulating layer (401a) and mounted on the circuit substrate (401c) (claim 15); and an inner via (404) that is provided in the insulating layer (401a) so as to make an electrical connection between wiring patterns (402) provided on different circuit substrates (401a, 401c),

Nakatani does not specific disclose a glass transition temperature Tg1 of the resin composition contained in the insulating layer (401b) and a glass transition temperature Tg2 of the resin of the insulating base material (401a; 401c) included in each of the circuit substrates satisfy a relationship Tg1 > Tg2.

Ozawa et al. teaches a wiring board as shown in figures 1-3 comprising a dielectric substrate (2, see column 3, lines 10-21) containing an inorganic filler and thermosetting resin formed between first and second resin substrates (6), the Tg of the dielectric substrate is higher than Tg of each of the resin substrates (because the dielectric substrate (2) contained a mixture of dielectric power and resin, and the resin substrate is just made by resin).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a teaching of Ozawa et al. employed in the module of Nakatani et al. in order to reduce stress and achieve excellent interconnection reliability.

As to claim 2, Nakatani et al. discloses a difference between the glass transition temperature Tg1 and the glass transition temperature Tg2 is at least 10^0C.

As to claim 3, Nakatani et al. discloses a plurality of the insulating layers are provided.

As to claim 4, Nakatani et al. discloses the insulating layer (401a) containing the inorganic filler in an amount of not less than 70% by weight and not more than 95% by weight, see column 11, lines 26-27.

As to claim 5, Nakatani et al. discloses the inorganic filler contains at least one selected from the group consisting of: Al_2O_3, MgO, BN, $Si0_2$, SiC, Si_3N_4, and AlN, see column 11, lines 24-25.

As to claim 6, Nakatani et al. discloses the thermosetting resin containing at least one selected from the group consisting of: an epoxy resin, a phenol resin, and an isocyanate resin, see column 11, lines 30-31.

As to claim 7, Nakatani et al. discloses the at least one electronic component comprises a semiconductor bare-chip, see column 11, lines 40-47.

As to claim 8, Nakatani discloses the inner via (404) is formed from a conductive resin composition, see column 11, lines 53-63.

As to claim 17, Nakatani discloses al of the limitations of the claimed invention (claim 1), except for no electric component formed in the circuit substrates.

Ozawa et al shows the wiring board comprising the resin substrate (6) with no component formed/housed in the substrate.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of Ozawa employed the module of Nakatani in order to reduce noise formed in a laminate layers

As to claims 9-14, Nakatani and Ozawa discloses all of the limitations of method of manufacturing an electronic component built-in module as shown in figures 1-6, and claims 1-8 does disclose all of the limitations of the final product of claimed language.

Response to Arguments

3. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Dinh
May 02, 2006.